Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1 - 26. (Canceled)

27. (Currently Amended) A data processing unit comprising:

an instruction cache to store instructions for execution, including instructions belonging to an M-bit instruction set and instructions belonging to an N-bit instruction set, where M < N;

an instruction fetch unit coupled to receive instructions from the instruction cache, and operable to produce control signals representative of decoded N-bit instructions; and

one or more execution units coupled to the receive the control signals from the instruction fetch unit,

the instruction fetch unit comprising a translation unit to translate an M-bit instruction received from the instruction cache to produce ~~one or more~~ N-bit instructions, at leas one M-bit instruction producing a sequence of N-bit instructions,

the instruction fetch unit further comprising a decoder unit to decode only N-bit instructions, thereby producing the control signals, the translation unit configured to deliver the ~~one or more~~ N-bit instructions to the decoder unit,

wherein the M-bit instruction set includes data instructions that produce results corresponding to M-bit ~~results~~ operations,

wherein the N-bit instruction set includes first data instructions that produce results corresponding to N-bit ~~results~~ operations and second data instructions that include N-bit instructions not otherwise needed for N-bit operation that emulate M-bit instructions to produce results corresponding to M-bit ~~results~~ operations,

wherein the instruction fetch unit is configured to produce one or more of the second data instructions in response to receiving an M-bit data instruction.

28. (Previously Presented) The data processor unit of claim 27 wherein the second data instructions further store the M-bit results into an N-bit data store and perform sign-extension of the M-bit result in the N-bit data store to produce an N-bit result.

29. (Previously Presented) The data processor unit of claim 27 wherein the instruction fetch unit includes a pre-decoder unit configured to receive N-bit instructions from the instruction cache and to produce one or more pre-decode signals in response to a received N-bit instruction, the pre-decoder unit providing a signal path to deliver the received N-bit instruction and the one or more pre-decode signals to the decoder, wherein the translation unit is further configured to produce corresponding pre-decode signals associated with the one or more N-bit instructions and to deliver the corresponding pre-decode signals to the decoder, wherein the corresponding pre-decode signals are pre-decode signals that would be produced if the one o more N-bit instructions were processed by the pre-decoder unit.

30. (Previously Presented) The data processor unit of claim 27 wherein M is 16, and N is 32.

31. (Currently Amended) A data processor comprising:

first means for caching instructions for execution, the instructions comprising instructions of an M-bit instruction set and instructions of an N-bit instruction set, where M < N;

second means for ~~decoding~~ translating M-bit instructions received from the first means to produce ~~one or more~~ N-bit instructions corresponding to an M-bit instruction, translation of at least one M-bit instruction producing a sequence of N-bit instructions upon translation;

third means for decoding N-bit instructions to produce control signals, wherein the N-bit instructions can be received from the first means or the second means; and

one or more execution units configured to receive the control signals, thereby executing the N-bit instructions,

wherein the M-bit instruction set includes M-bit data instructions, and ~~for operating on M-bit data,~~

wherein the N-bit instruction set comprises first data instructions ~~for operating on~~ corresponding to N-bit instructions ~~data~~ and second data instructions ~~for operating on~~ corresponding to M-bit instructions ~~data~~, the second data instructions including N-bit instructions not otherwise needed for N-bit operation that emulate M-bit operation to produce results corresponding to M-bit operation.

32. (Previously Presented) The data processor of claim 31 wherein the data instructions in the M-bit instruction set produce M-bit results, wherein the first data instructions of the N-bit instruction set produce N-bit results, and wherein the first data instructions of the N-bit instruction set produce M-bit results.

33. (Previously Presented) The data processor of claim 32 wherein the second means is further for producing one or more of the second data instructions of the N-bit instruction set in response to receiving a data instruction from the M-bit instruction set.

34. (Previously Presented) The data processor of claim 31 wherein the second means is further for producing first pre-decode signals associated with the one or more N-bit instructions, wherein the third means comprises a decoder means for producing the control signals and a pre-decoder means for producing second pre-decode signals, wherein the decoder means is responsive to the first pre-decode signals and to the second pre-decode signals.

35. (Previously Presented) The data processor of claim 31 wherein M is 16 and N is 32.

36. (Currently Amended) A microprocessor comprising:

a memory for storing instructions, the instructions comprising M-bit instructions and N-bit instructions, where $M < N$;

a translation circuit for receiving M-bit instructions from the memory, the translation circuit configured to produce ~~one or more~~ N-bit instructions in response to a received M-bit instruction and to produce corresponding pre-decode signals associated with the ~~one or~~

~~more~~ N-bit instructions, at least one M-bit instructions producing a sequence of N-bit instructions upon translation;

a predecoder circuit for receiving N-bit instructions from the memory, the predecoder circuit configured to produce associated pre-decode signals in response to a received N-bit instruction; and

a decoder circuit for receiving the ~~one or more~~ N-bit instructions and the corresponding pre-decode signals from the translation circuit and further for receiving the received N-bit instruction and the associated pre-decode signal from the predecoder circuit, wherein control signals are produced in response thereto,

wherein the pre-decode signals corresponding to the ~~one or more~~ N-bit instructions that are produced by the translation circuit are the same pre-decode signals that would be produced if the ~~one or more~~ N-bit instructions were received by the predecoder circuit, and

wherein the N-bit instructions include N-bit instructions not otherwise needed for N-bit operation that emulate M-bit instructions in order to produce results corresponding to M-bit operation.

37. (Currently Amended) The microprocessor of claim 36 wherein ~~the N-bit instructions include first data instructions for processing N-bit data and second data instructions for processing M-bit data, wherein~~ one or more of the second data instructions are produced by the translation circuit in response to receiving an M-bit instruction that is a data instruction.

38. (Previously Presented) The microprocessor of claim 37 wherein the second data instructions produce M-bit results.

39. (Previously Presented) The microprocessor of claim 38 wherein the second data instructions further store the M-bit results in an N-bit data store and perform a sign-extension operation to produce an N-bit result.

40. (Previously Presented) The microprocessor of claim 36 wherein M is 16 and N is 32.